



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,926	02/11/2004	Takahiro Yamaguchi	02008/092002	2381
7590	12/20/2007		EXAMINER	
Jonathan P. Osha ROSENTHAL & OSHA L.L.P. Suite 2800 1221 McKinney St. Houston, TX 77010			BAYARD, EMMANUEL	
			ART UNIT	PAPER NUMBER
			2611	
			MAIL DATE	DELIVERY MODE
			12/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/776,926	YAMAGUCHI ET AL.
Examiner	Art Unit	
Emmanuel Bayard	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 15 October 2007.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) _____ is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 39-52 is/are allowed.
- 6) Claim(s) 1-15, 19-28 and 36-38 is/are rejected.
- 7) Claim(s) 16-18 and 29-35 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) Notice of Informal Patent Application
- 6) Other: _____

DETAILED ACTION

This is in response to amendment filed on 10/15/07 in which claims 1-53 are pending. the applicant's arguments have been fully considered but they are not persuasive enough. Therefore this case is made final. (see Examiner response to arguments below).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Gauthier et al U.S. patent No 6,671,863 B2.

As per claim 1, Gauthier teaches measuring apparatus for measuring jitter transfer function of an electronic device, comprising: a timing jitter estimator operable to calculate an output timing jitter sequence of an output signal based on said output signal output (see figs. 5a-5b, 8 and abstract and col.1, lines 65-67 and col.2, lines 64-67 and col.3, lines 7-10 and col.9, lines 18-20, 48-50) a from said electronic device (see col.1, line 31); and a jitter transfer function estimator (col.5, lines 25-37) operable to calculate jitter transfer function of said electronic device based on said output timing jitter Sequence.

As per claims 19-20, Gauthier et al does teach Wherein said timing jitter estimator estimates timing jitter sequence of input data clock signal for generating input data signal given to said electronic device, and a timing jitter sequence of output data signal output from said electronic device in response to said input data signal, and said jitter transfer function measuring apparatus measures a jitter transfer function between said input data signal and said output data signal based on said timing jitter sequence estimated by said timing jitter estimator (see rejection of claim 1 above).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gauthier et al U.S. Patent No 6,671,863 B2 in view of Yang U.S. patent No 6,573,940 B1.

As per claim 2, Gauthier et al teaches all the features of the claimed invention except an instantaneous phase noise estimator operable calculate an instantaneous phase noise of said output signal based on said output signal; and a re-sampler operable to generate said output timing jitter sequence obtained by re-sampling said instantaneous phase noise at predetermined timings.

Yang teaches an instantaneous phase noise estimator operable calculate an instantaneous phase noise of said output signal based on said output signal (see col.23, lines 15-60); and a re-sampler operable to generate said output timing jitter sequence obtained by re-sampling said instantaneous phase noise at predetermined timings (see col.23, lines 15-60).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Yang into Gauthier as to acquire higher quality video signals as taught by Yang (see col.23, line 40).

As per claim 3, Yang teaches a re-sampler re-samples said instantaneous phase noise (see col.23, lines 15-63). Furthermore implementing such teaching into Gauthier at timings approximately same as zero-crossing timings of said output signal would have been obvious to one skilled in the art as to acquire higher quality video signals as taught by Yang (see col.23, line 40).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 4-15, 21-24, 36, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gauthier et al U.S. Patent No 6,671,863 B2 in view of Choudhary U.S. patent No 6,782,404 B2.

As per claims 4-5, Gauthier teaches all the features of the claimed invention except receiving a plurality of input signals having and outputs a plurality of said output signals to respectively corresponding input signals.

Choudhary teaches A measuring apparatus as claimed in claim 1, wherein said electronic device receives a plurality of input signals having different jitter amounts and outputs said plurality of output signals respectively corresponding to said plurality of input signals, (see abstract and figs.7, 10 and col.2, lines 12-25 and col.4, lines 32-35 and col.7, lines 30-55) said timing jitter estimator calculates said output timing jitter sequences corresponding to said output signals respectively, and said jitter transfer function estimator calculates said jitter transfer function further based on said information indicating a plurality of input timing jitter sequences (see fig.7).

It would have been obvious to one of ordinary skill in the art to incorporated the teaching of Choudhary et al into Gauthier as to provide a jitter tolerant system which users could program by supplying appropriate values to eliminate noise effects as taught by Choudhary (see col.7, lines 34-40).

As per claim 6, Gauthier teaches a frequency-domain (see col.2, line 9). Furthermore implementing such teaching in combination with Choudhary as to

transform said input timing jitter sequences and said output timing jitter sequences to frequency domain signals would have been obvious to one skilled in the art as to provide a jitter tolerant system which users could program by supplying appropriate values to eliminate noise effects as taught by Choudhary (see col.7, lines 34-40).

As per claims 7, 8, 10-11, Gauthier teaches jitter transfer function estimator comprises jitter gain estimator operable to calculate a gain ($H_j(f)$) of said jitter transfer function (see col.5, lines 17-37). Furthermore implementing such gain to generate the following Equation would have been obvious to one skilled in the art as to optimize the PLL loop bandwidth related to balancing the effect of input jitter with the PLL loop's speed of response to compensate for output jitter induced by power supply noise.

As per claim 9, Gauthier teaches wherein said jitter gain estimator calculates said gain of said jitter transfer function based on a result of linear fitting relationship between a peak-to-peak value of an input timing jitter (see col.4, lines 24-25 and col.5, lines 17-50). Furthermore implementing such gain to and peak-peak value of said plurality of input timing jitter sequences to generate an output timing jitter of said plurality of output timing jitter sequences, or a root-mean-square (RMS) value of said output timing jitter said output timing jitter sequences and a root -mean-square value of an input timing jitter of said plurality of input timing jitter sequences would have been obvious to one skilled in the art as to optimize the PLL loop bandwidth related to balancing the effect of input jitter with the PLL loop's speed of response to compensate for output jitter induced by power supply noise.

As per claim 12, would include wherein said jitter applying unit applies a sinusoidal jitter to said input signal as said input timing jitter . as to optimize the PLL loop bandwidth related to balancing the effect of input jitter with the PLL loop's speed of response to compensate for output jitter induced by power supply noise.

As per claim 13, Gauthier would include wherein said jitter applying unit applies said input timing jitter by modulating a phase of said input signal as to optimize the PLL loop bandwidth related to balancing the effect of input jitter with the PLL loop's speed of response to compensate for output jitter induced by power supply noise.

As per claim 14, wherein said jitter applying unit applies said input timing jitter by modulating frequency of said input signal as to optimize the PLL loop bandwidth related to balancing the effect of input jitter with the PLL loop's speed of response to compensate for output jitter induced by power supply noise.

As per claims 15 and 21-22, Choudhary teaches a clock recovery unit operable to generate a recovered clock signal of said output signal based on said output signal, wherein said timing jitter estimator estimates said output (see fig.7). Furthermore implementing such teaching into Gauthier as to generate accurate time synchronization throughout the network.

As per claims 23-24, Choudhary teaches receives serial data as said input data, and outputs a parallel data (see fig.7) Furthermore implementing such teaching into Gauthier for generating output data signal from output pins , the number of output pins being predetermined, said timing jitter estimator estimates said output timing jitter sequence of said output data signal according to data output from a certain output pin

out of said output pins, and said input unit supplies said input data signal to said electronic device, in which a bit of the pattern data corresponding to the certain output pin out of said output pins repeats 1 (high) and 0 (low) by turns as to optimize the PLL loop bandwidth related to balancing the effect of input jitter with the PLL loop's speed of response to compensate for output jitter induced by power supply noise.

As per claim 36, Gauthier teaches a measuring apparatus for measuring jitter transfer function of an electronic device, comprising: a timing jitter estimator operable to calculate an output timing jitter sequence of an output signal based on said output signal output (see figs. 5a-5b, 8 and abstract and col.1, lines 65-67 and col.2, lines 64-67 and col.3, lines 7-10 and col.9, lines 18-20, 48-50) a from said electronic device (see col.1, line 31); and a jitter transfer function estimator (col.5, lines 25-37) operable to calculate jitter transfer function of said electronic device based on said output timing jitter Sequence.

However Gauthier does not teach receiving a plurality of input signals having and outputs a plurality of said output signals to respectively corresponding input signals.

Choudhary teaches A measuring apparatus as claimed in claim 1, wherein said electronic device receives a plurality of input signals having different jitter amounts and outputs said plurality of output signals respectively corresponding to said plurality of input signals, (see abstract and figs.7, 10 and col.2, lines 12-25 and col.4, lines 32-35 and col.7, lines 30-55) said timing jitter estimator calculates said output timing jitter sequences corresponding to said output signals respectively, and said jitter transfer function estimator calculates said jitter transfer function further based on said information indicating a plurality of input timing jitter sequences (see fig.7).

It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Choudhary et al into Gauthier as to provide a jitter tolerant system which users could program by supplying appropriate values to eliminate noise effects as taught by Choudhary (see col.7, lines 34-40).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 25-26 and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Dalmia et al U.S. patent No 5,835,501.

2. As per claims 25 and 37, Dalmia et al teaches a measuring apparatus for measuring a bit error rate of device, comprising a bit error rate estimator operable to estimate said bit error rate (see figs. 2 and 4 element 3 and col.3, lines 13-15) of said device based on a gain of jitter transfer function of said device (see fig.3 and col.2, lines 33-52 and col.3, lines 33-40 and col.6, lines 6-9, 48 and col.7, lines 15-21) measuring the bit error rate based on an IC circuit is the same as the claimed (electronic device) (see col.4, lines 54-67 and col.5, lines 24-40).

As per claim 26, Dalmia does teach wherein said bit error rate estimator estimates said bit error rate further based on a phase of said jitter transfer function (see col.3, line 22).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 27-28 and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Dalmia U.S. Patent no 5,835,501.

3. As per claims 27 and 38, Dalmia teaches a measuring apparatus for measuring jitter tolerance of an electronic device, comprising a jitter tolerance estimator operable to estimate said jitter tolerance of said device based on a gain of jitter transfer function of said device (see col.2., lines 26-35, 45-52 and col.3, line 33-40 and col.4, lines 21-27, 64-67) the jitter tolerance based on an IC circuit is the same as the claimed (electronic device) (see col.4, lines 54-67 and col.5, lines 24-40).

As per claim 28, Dalmia inherently teach wherein said jitter tolerance estimator estimates said jitter tolerance further based on a phase of said jitter transfer function. It is well Known in the art that unwanted phase movement is Known as "jitter" which can determined the phase difference between the input signal and the output signal. Also the output jitter divided by the input jitter or the input to output transfer characteristic of

a PLL is known as "jitter transfer function". This transfer function has a "low pass" characteristics and it is generally desirable to make the cut off frequency as low as possible. Therefore Dalmia inherently teach the claimed limitation

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gauthier et al U.S. Patent No 6,671,863 B2 in view of by Eubanks U.S. Pub 2003/0063701 A1.

As per claim 53, Gauthier teaches measuring apparatus for measuring jitter transfer function of an electronic device, comprising: a timing jitter estimator operable to estimate an output timing jitter sequence of an output signal based on said output signal output (see figs. 5a-5b, 8 and abstract and col.1, lines 65-67 and col.2, lines 64-67 and col.3, lines 7-10 and col.9, lines 18-20, 48-50) a from said electronic device (see col.1, line 31); and a jitter transfer function measuring (col.5, lines 25-37) operable to measure jitter transfer function of said electronic device based on said output timing jitter Sequence.

However Gauthier does not teach a timing jitter estimator to estimating an output instantaneous phase noise and to measure a jitter transfer function based on said instantaneous phase noise.

Eubanks et al teaches a timing jitter estimator to estimating an output instantaneous phase noise and to measure a jitter transfer function based on said

instantaneous phase noise (see figs. 2-4, 8 and page 2, paragraph [0031] and page 3 paragraph [0046] and page 5, paragraph [0089]).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Eubanks into Gauthier as to correctly filter out the jitter from the clock to allow the clock to be used as a system clock as taught by Eubanks (see abstract and page 3, paragraph [0046]).

Response to Arguments

1. Applicant's arguments filed 10/15/07 have been fully considered but they are not persuasive. In page 3 paragraph 4 and page 4 of the response, applicant asserts that Gauthier does not teach a timing jitter estimator operable to calculate an output timing jitter sequence of an output signal based on said output signal output (see figs. 5a-5b, 8 and abstract and col.1, lines 65-67 and col.9, lines 18-20, 48-50) a from said electronic device (see col.1, line 31); and a jitter transfer function estimator (col.5, lines 25-37) operable to calculate jitter transfer function of said electronic device based on said output timing jitter Sequence.
2. Examiner respectfully disagrees. In fact Gauthier teaches estimate jitter of the PLL (see and col.2, lines 64-67 and col.3, lines 7-10) and a jitter transfer function estimator (col.5, lines 25-37) operable to calculate jitter transfer function of said electronic device based on said output timing jitter Sequence. It is well Known in the art that unwanted phase movement is Known as "jitter" which can determined the phase difference between the input signal and the output signal. Also the output jitter divided

by the input jitter or the input to output transfer characteristic of a PLL is known as "jitter" transfer function". This transfer function has a "low pass" characteristics and it is generally desirable to make the cut off frequency as low as possible. Gauthier teaches all the claim limitation as mentioned above therefore applicant's arguments are moot and this case stand rejected as stated in this final office action.

3. In page 5, paragraph 2 of the response, applicant asserts that Yang is silent to at least the timing jitter estimator and jitter transfer function.

4. Examiner respectfully disagrees. In fact fig.9a of Yang shows a PLL(824) which it is well Known in the art to calculate unwanted phase movement Known as "jitter" which can determined the phase difference between the input signal and the output signal. Also the output jitter divided by the input jitter or the input to output transfer characteristic of a PLL is known as "jitter transfer function". This transfer function has a "low pass" characteristics and it is generally desirable to make the cut off frequency as low as possible. Since Yang teaches the above limitations, applicant's arguments are moot and this case stand rejected as stated in this final office action.

5. In page 6, paragraph 2 of the response, applicant asserts that Choudhary is silent to at least the timing jitter estimator and jitter transfer function.

6. Examiner respectfully disagrees. In fact col.1, lines 35-37 and col.3, lines 30-32 of Choudhary recite a PLL. A PLL it is well Known in the art to calculate unwanted phase movement Known as "jitter" which can determined the phase difference between the input signal and the output signal. Also the output jitter divided by the input jitter or the input to output transfer characteristic of a PLL is known as "jitter transfer function".

This transfer function has a “low pass” characteristics and it is generally desirable to make the cut off frequency as low as possible. Since Choudhary teaches the above limitations, applicant’s arguments are moot and this case stand rejected as stated in this final office action.

7. In page 7, paragraph 1 of the response, applicant asserts that Dalmia does not teach a bit error rate based on a jitter transfer function

8. Examiner respectfully disagrees. In fact Dalmia teaches a BER (See fig.2 element 3) having an input coupled to a PLL (see figs.2-3 element 6) . A PLL it is well Known in the art to calculate unwanted phase movement Known as “jitter” which can determined the phase difference between the input signal and the output signal. Also the output jitter divided by the input jitter or the input to output transfer characteristic of a PLL is known as “jitter transfer function”. This transfer function has a “low pass” characteristics and it is generally desirable to make the cut off frequency as low as possible. Since Dalmia teaches the above limitations, applicant’s arguments are moot and this case stand rejected as stated in this final office action.

Allowable Subject Matter

9. Claims 16-18, 29-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 39-52 are allowed.

11. The following is a statement of reasons for the indication of allowable subject matter: The recited prior arts fail to anticipate or render obvious the following recited

features: An analytic signal transformer operable to transform said output signal to complex analytic signal; an instantaneous phase estimator operable to estimate an instantaneous phase of said analytic signal based on said analytic signal; a linear instantaneous phase estimator operable to estimate a linear instantaneous phase of said output signal based on an instantaneous phase of said analytic signal as recited in claim 16. An analytic signal transformer operable to transform said output signal to complex analytic signal; an instantaneous phase estimator operable to estimate an instantaneous phase of said analytic signal based on said analytic signal as recited in claim 33. A jitter related transmission penalty estimator operable to estimate said reliability of said electronic device against jitter based on said jitter distortion as recited in claim 38. A jitter distortion estimator operable to estimate jitter distortion of an output timing jitter of said output signal output from said electronic device according to said first check signal, against an ideal timing jitter of said output signal which said electronic device is to output according to said first check signal; and a judging unit operable to judge whether said jitter tolerance is a right value based on said jitter distortion as recited in claim 57.

12.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
14. Cupo U.S. patent no 5,115,452 teaches phase jitter.

15. Wong U.S. Patent no 6,697,445 teaches a method and apparatus with enhanced jitter.

Bulzachelli U.S. Patent No 5,036,298 teaches a clock recovery.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571 272 3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

12/17/2007

Emmanuel Bayard

Primary Examiner

EMMANUEL BAYARD
PRIMARY EXAMINER

16.